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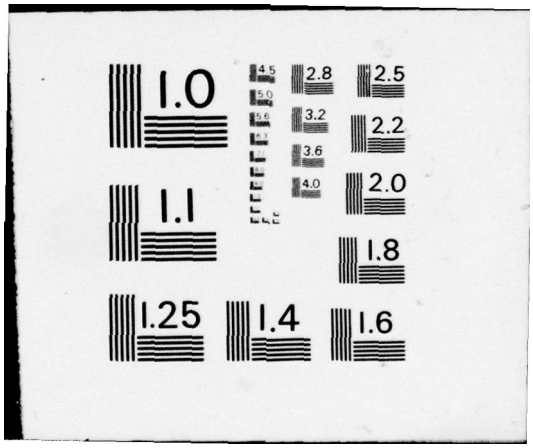
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AUTOMATIC CRACK MEASUREMENT SYSTEM

BENET WEAPONS LABORATORY
WATERVLIET ARSENAL
WATERVLIET, N.Y. 12189

APRIL 1975

TECHNICAL REPORT

AMCMS No. 539.0M.6350

Pron No. M7-3-P4539-01-M7-M7

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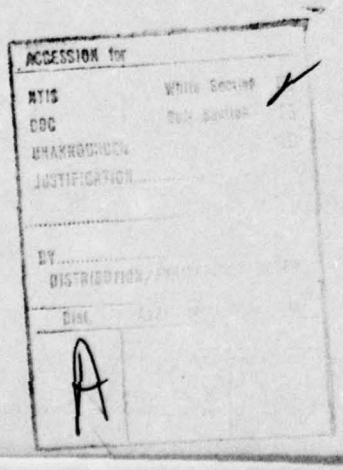

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REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER: (14) WVT-TR-75018
2. GOVT ACCESSION NO.
3. RECIPIENT'S CATALOG NUMBER

4. TITLE (and Subtitle): (6) AUTOMATIC CRACK MEASUREMENT SYSTEM.
5. TYPE OF REPORT & PERIOD COVERED: (9) Technical rept.
6. PERFORMING ORG. REPORT NUMBER

7. AUTHOR(s): (10) Donald C. Winters
8. CONTRACT OR GRANT NUMBER(s)

9. PERFORMING ORGANIZATION NAME AND ADDRESS
Benet Weapons Laboratory
Watervliet Arsenal, Watervliet, N.Y. 12189
SARWV-RDT
10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: (16) AMCMS No. 539-0M.6350
Pron No. -M7-3-P4539-01-M7-M7

11. CONTROLLING OFFICE NAME AND ADDRESS
US Army Armament Command
Rock Island, IL 61201
12. REPORT DATE: (11) April 1975
13. NUMBER OF PAGES: 24

14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office): (12) 25p.
15. SECURITY CLASS. (of this report): Unclassified
15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Ultrasonics
Cracks
Subtractor
Comparator
Circuitry

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Previous work has resulted in an automatic crack tip distance measurement circuit. An operator minimizes this distance and pushes a "record" switch which stores the crack position and depth data on magnetic tape. The Hill Climbing Circuits described in this report perform that operation automatically. These circuits are described in sufficient detail to be duplicated. Included in the design are an electronic binary-coded-decimal subtractor, a comparator, storage registers, and control circuits all using integrated circuits.

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AUTOMATIC CRACK MEASUREMENT SYSTEM

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APRIL 1975

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INTRODUCTION

Previous work under the MTT program and described in Watervliet Arsenal Report WVT 7248, September 1972 has resulted in an automatic crack tip distance measurement circuit, i.e. a circuit which computes the distance from the probe to the crack tip. This report covers circuit design which is a continuation of the earlier work. The two reports taken together constitute a complete description of the ultrasonic system. Crack depth is the distance from the bore, where the crack originates, to the tip. When a crack has been located and optimized for minimum crack tip distance, the operator pushes a "record" switch and the crack location and depth are recorded on a Data Acquisition System (DAS).

The circuits described in this report (Hill Climbing Circuits) make the operator decision when to record and automatically send out a "record" signal to the DAS. Construction details and complete wiring diagrams are furnished. The diagram of the Crack Tip Measurement Circuit as modified to work with the "Hill Climbing Circuit" is included for completeness.

BACKGROUND

Thick-walled cylinders, exposed to repeated cycles of high internal pressure, may fail by low-cycle fatigue. The fatigue life of these cylinders is primarily a function of the crack propagation rate. The portion of fatigue life consumed in crack initiation may be considered an additional safety factor. To develop design criteria and

to set safe inspection standards, it is necessary to know not only the length, but the depth and shape of fatigue cracks.

A technique has been developed for the accurate end-on measurement of crack depth in thick-walled cylinders using a straight-beam ultrasonic probe. This technique has proved useful not only under laboratory conditions, but also in practical situations such as inspection of cannon tubes after firing.

In the presence of multiple cracks, the measurement, recording and analysis of all the factors of fatigue crack growth can be quite complicated. To alleviate this problem, a system for the rapid collection, reduction, and analysis of this data by computer has been developed. The resulting measuring devices, the data acquisition system and the link to an IBM 360 computer are described in reference 1.

Crack location and orientation are measured by a locator which has been designed to provide digital position data while operating on the surface of a cylinder (breech of the cannon). Crack tip distance is measured electronically using integrated circuits. A data acquisition system has been designed to scan the binary coded decimal transducer outputs, format the data, and record on IBM compatible magnetic tape.

GENERAL SYSTEM DESCRIPTION

The automatic crack measurement system is shown in Figure 1.

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[1] Winters, Donald C., "Automated Crack Position and Depth Measurements on Cannon Tubes", Watervliet Arsenal Technical Report WVT-7248, September 1972.

Shown on the left attached to the cannon breech by magnets is the locator. The ultrasonic flaw detector is in the center on the tool cart. The Data Acquisition System (DAS) is on the right. The crack tip measurement circuitry is in the card rack directly over the flaw detector. The "Hill Climbing" Circuits, to be described in detail in this report, are in the card rack directly over the crack tip measurement circuits.

The "Hill Climbing" circuits are decision circuits which operate on the binary-coded-decimal crack tip numbers coming from the measuring circuits. The number is the distance, in hundredths of an inch, from the probe, resting on the cannon outer surface, to the crack tip. These circuits make the decision as to when the probe is directly over the crack.

The input numbers are updated continuously at the repetition rate of the flaw detector. The rate ranges from 80 to 2000 pulses per second but is usually operated at about 1000 pps. The numbers are in the form of voltages. +5 volts represents a ONE, and 0 volts a ZERO. These voltages only change when the crack tip distance changes.

If there is no crack, this number represents the distance to the back wall (the inside diameter (ID) of the cannon). The back wall distance is dialed in by means of three thumb-wheel switches which are also coded in binary-coded decimal form. This number is continuously subtracted from the crack tip distance number and the difference is the actual crack depth measured from the ID.

The crack depth number is sampled twenty times per second. The

rate is controlled by a local oscillator and determined by the probe rate of travel over the cannon surface. The sampled crack depth readings are stored in Register A. See Figure 2, the block diagram of the Hill Climbing circuit. One twentieth of a second later, the next sampled crack depth reading is stored in Register A. A is now compared with register B. B contains the previous reading of A. If A is larger than B, a flip-flop circuit is set to HIGH or ONE. If each successive sampled value stored in A is larger than its previous value continued set signals indicating A > B cause the flip-flop to remain HIGH. The first B > A signal resets the flip-flop. The negative going flip-flop output voltage fires a one-shot multivibrator which transfers the contents of B to an output register. The output register now contains the maximum value of crack depth.

The multivibrator output is widened and, if not inhibited by a previous uncompleted data transfer, causes a "read out" pulse to transfer the maximum crack depth out to the DAS while at the same time reading the coordinates of the probe location into the DAS.

The control circuitry consists of a chain of one-shot multivibrators arranged to provide a sequence of control signals about 5 microseconds apart. These signals shift the numbers from the subtractor to register A to register B to the output register and perform the comparisons.

SUBTRACTOR

Subtraction of sign plus tens complement (8421 BCD) code numbers can be performed in the following manner. See reference 2 for additional information. Consider the subtraction of two digits M (minuend) and S (subtrahend):

$$M - S = M_8M_4M_2M_1 - S_8S_4S_2S_1$$

now complementing the bits of S gives

$$\overline{S}_8\overline{S}_4\overline{S}_2\overline{S}_1 = 1111 - S_8S_4S_2S_1$$

where the expression on the right represents a binary subtraction. Consquently

$$M - S = M_8M_4M_2M_1 + \overline{S}_8\overline{S}_4\overline{S}_2\overline{S}_1 - 1111, \text{ or}$$

$$M - S = M_8M_4M_2M_1 + \overline{S}_8\overline{S}_4\overline{S}_2\overline{S}_1 + 0001 - 10000$$

This says that M - S can be formed through the binary addition of $M_8M_4M_2M_1$, $\overline{S}_8\overline{S}_4\overline{S}_2\overline{S}_1$, and 1. If the addition overflows (i.e. if a 1 results in the fifth bit position) then the first 4 bits provide the correct representation for the difference as an 8421 BCD Code digit. On the other hand, if the addition does not overflow, then the subtrahend digit was greater than the minuend digit and two things must be done.

This result must be corrected, and a borrow must be propagated to the next digit position by not adding the extra 1 into that addition.

---

[2]Peatman, John B., "The Design of Digital Systems", Pages 343-346, McGraw-Hill.

A result of 1111 should be 1001, 1110 should be 1000, etc. This can be corrected by adding 11001-1111 = 1010 to the result and neglecting the carry which occurs.

The complete circuit in block diagram form is shown in Figure 3. The ONE is added in at the carry-in input of the first full adder, which is one of four in the integrated circuit (IC) package SN 7483.

All of the integrated circuits comprising the subtractor are mounted on board 1 shown in Figure 4. The inter-package and inter-board wiring are shown in Figure 5. The connectors into which the boards plug have 40 terminals on the back. Pin 1 is ground and 40 is +5V. The numbers with the arrows pointing away apply to that board connector.

A picture of the back board wiring is shown in Figure 6. The front panel layout of the card rack is shown in Figure 7. On the left is the green Light Emitting Diode (LED) characters continuously displaying the results from the subtraction circuits. On the right of the front panel are the thumb wheel switches for inserting the back-wall distance reading M.

COMPARATOR

The comparator circuits and their two associated registers, Register "A" and Register "B", are located on Board 2 of Figure 4. Figure 8 is a photograph of this board. The SN 7485 integrated circuits are each a 4 bit magnitude comparator. Reference 3 gives the

[3]Integrated Circuits Catalog for Design Engineers, Texas Instruments, Inc., Section 9, Pages 286-288.

truth-table for them. There are three of these, one for each decimal digit.

The comparator operates on a voltage level input on each of its 11 input lines. The settling time for a change in inputs to a change in output is about 20 nanoseconds.

Level outputs from A > B and A < B terminals are used. These go to a coincidence circuit, are strobed at the appropriate time by the sequencing circuits, and the strobed output is used to set or reset a flip-flop. The output of this flip-flop can be seen on Test Point (TP) G of Figure 2. The same test points appear by the same letters in all of the diagram figures.

CONTROL

The control circuits are made up of one-shot monostable multivibrators SN74121. The control sequence is initiated by the sampling circuit free-running blocking oscillator MV II & III in the automatic mode.

This oscillator, consisting of two monostable multivibrators connected tail-to-mouth, doesn't always start when power is applied. This is a condition which needs remedying in the next design, but for the present a quick fix was to connect a push button switch from ground to Input B of MV III to momentarily ground B. As B goes positive, due to being tied to $\overline{Q}$ of MV II, the multivibrator action starts, causing $\overline{Q}$ of MV III to go to ground for its timed interval. When $\overline{Q}$ goes positive again at the end of this interval, input B of MV II which is connected to $\overline{Q}$ of MV III causes $\overline{Q}$ of MV II to go to

ground. The two multivibrators continue to turn each other on indefinitely. The advantage of this circuit is that it can be made using SN74121s like the rest of the control circuits and these are available, voltage compatible, and easily mounted.

The mode switch S_1 is on the front panel. In its manual position, the control sequence is initiated by an external record switch which grounds the B input of MV I (see Figure 2). S_1 takes either the output of MV I or of MV II-III to MV IV on the B input. The A input of MV IV comes from the original distance readout circuits via the Amphenol input cable. The output of MV IV occurs on the first transfer pulse after the sampling signal, and can be seen by connecting an oscilloscope to Test Point C. Figure 9 shows the timing of the control sequence. There is a signal at TP C only if the ultrasonic probe is resting on a cannon or test block.

The Q output of MV V is seen at TP D as a positive going pulse 5 micro seconds (μS) long. The output of the subtractor is wired to the input of Register "A", composed of SN 7475 integrated circuits and to the LED green display. The trailing edge (negative going) of the signal from Q of MV V strobes the subtractor results into register A at a time 5 μS after the transfer pulse from TP 11 of the crack tip distance circuits.

MV VI inserts a second 5 μS delay. The Q output from MV VII is used to strobe the comparator results (Register A compared to Register B) into the flip-flop (FF). The comparator output is a voltage level which is connected to one input of a NAND Gate (SN 7400) the other

input has the Q output from MV VII connected to it. The output of the NAND only goes low when there is a coincidence of comparator output high and MV VII output Q high.

The negative edge sets the FF 10 μS after transfer pulse from TP 11. This signal can be seen on TP E.

The FF is made up from two NAND gates tied tail-to-mouth. It is a set-reset FF only.

When the FF re-sets, it triggers MV IX which transfers contents of B register to the output register. The peak value of crack depth is stored in B at this time. The output register is composed of 3 SN 7475 integrated circuits (IC). To provide power to drive the DAS inputs, three SN 7407 interface buffer ICs were used between the output register and DAS.

MV IX provides another 5 μS delay and then MV X is fired to transfer the content of the output register to the DAS.

The last event in the sequence in automatic mode is to transfer the contents of A register to B register in readiness for the next sequence. The trailing edge of the Q output of MV VIII does this.

In the manual mode of operation, one more event in the sequence occurs as MV VIIIA fires, transfers B to the output, and provides a record pulse to the DAS.

SUMMARY

A prototype system of the entire crack depth reading circuitry has been constructed, debugged, tested, and demonstrated. The circuitry has been interfaced with the Data Acquisition System and

the automatic recording of data sets accomplished when manually moving the ultrasonic probe over a cannon section with cracks in it.

Crack depth is read to an accuracy of $\pm$ 0.030", initially, and subsequent changes in depth to 0.010".

All wiring diagrams and a timing diagram are included in this report. Figure 10 is similar to Figure 4 and Figure 5, but does not carry board or connector numbers. It is included so that the circuits can be duplicated electrically but with a different physical layout. The physical layout is shown in Figures 1, 6, 7, and 8. They are included so a physical duplicate could be constructed if desired. Figure 11 is the original crack tip measurement circuits wiring diagram done under previous PEMA funding as modified to permit connection to the Hill Climbing circuit.

REFERENCES

1. Winters, Donald C., "Automated Crack Position and Depth Measurements on Cannon Tubes", Watervliet Arsenal Technical Report WVT-7248, September 1972.
2. Peatman, John B., "The Design of Digital Systems", Pages 343-346, McGraw-Hill.
3. Integrated Circuits Catalog for Design Engineers, Texas Instruments, Inc., Section 9, Pages 286-288.

Figure 1. Photograph of crack measurement system.

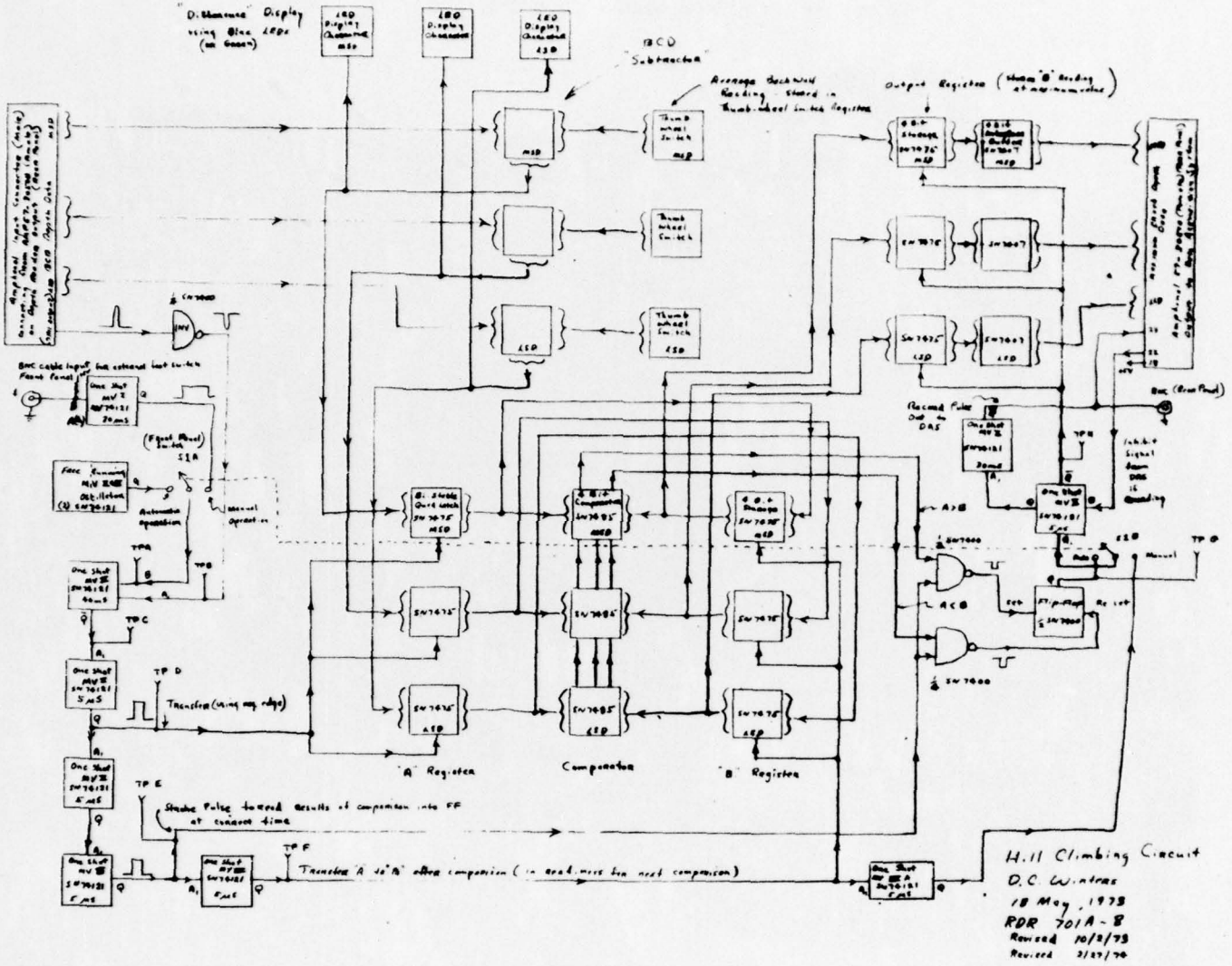

Figure 2. Block diagram of Hill Climbing Circuit.

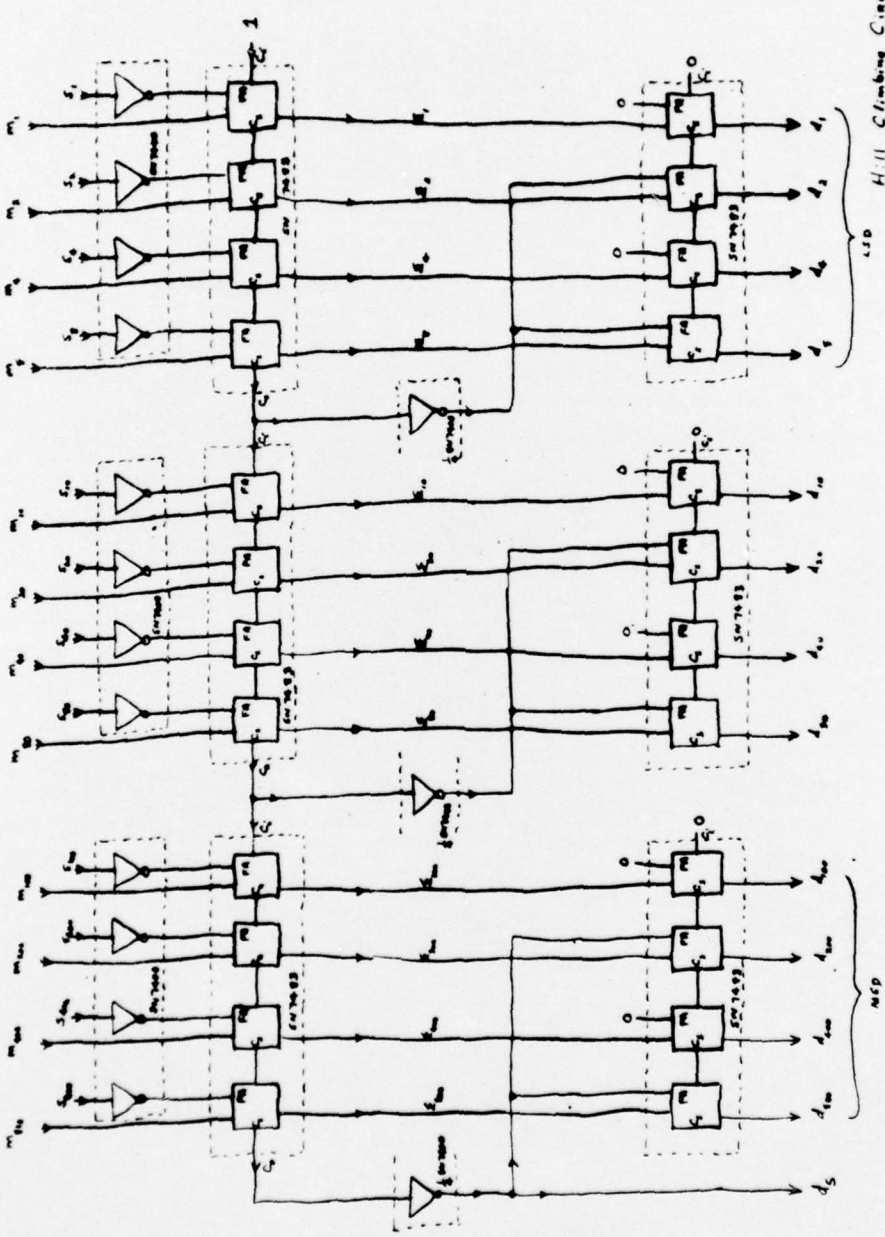

Figure 3. Block diagram of BCD Subtractor

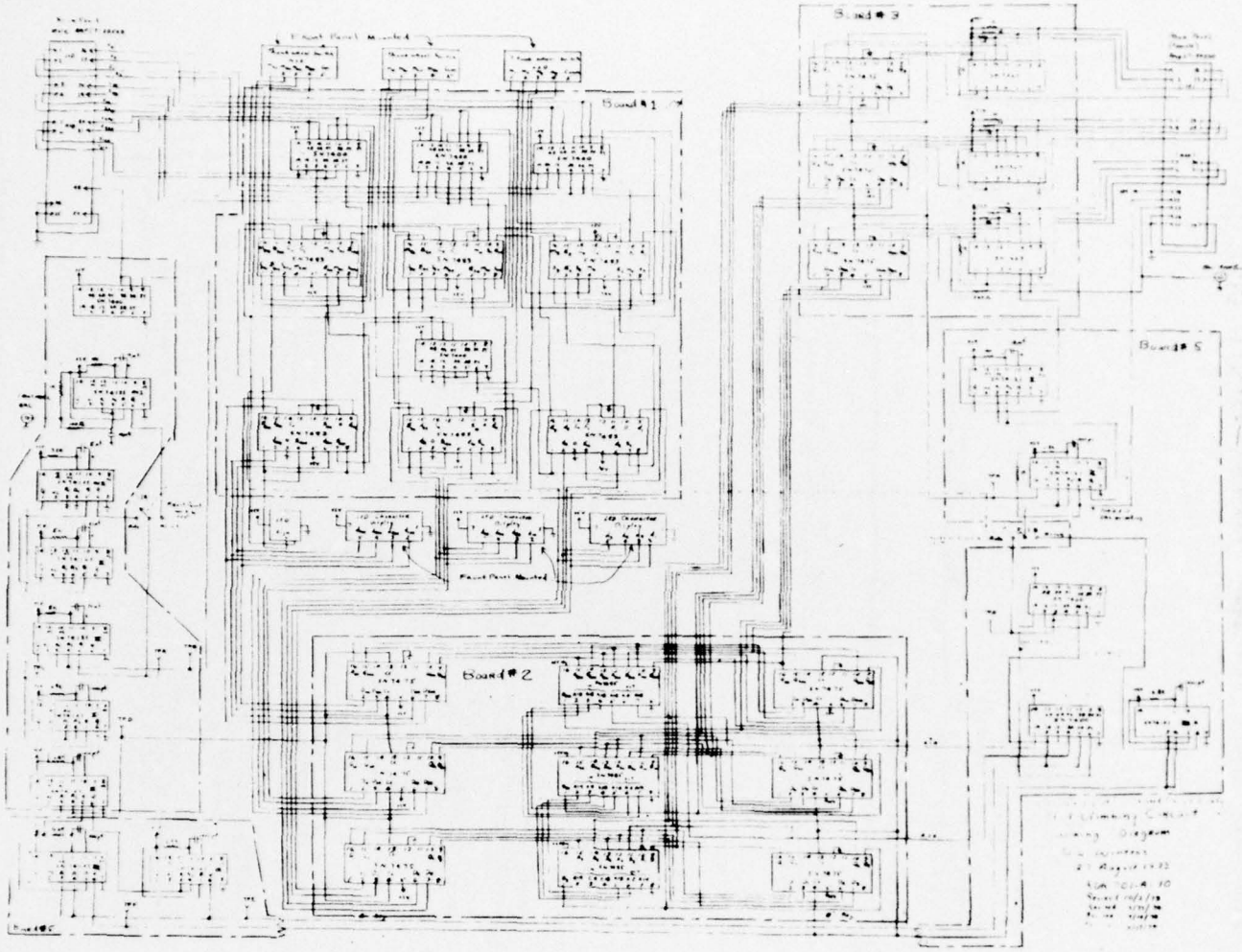

Figure 4. Circuit division by printed circuit boards.

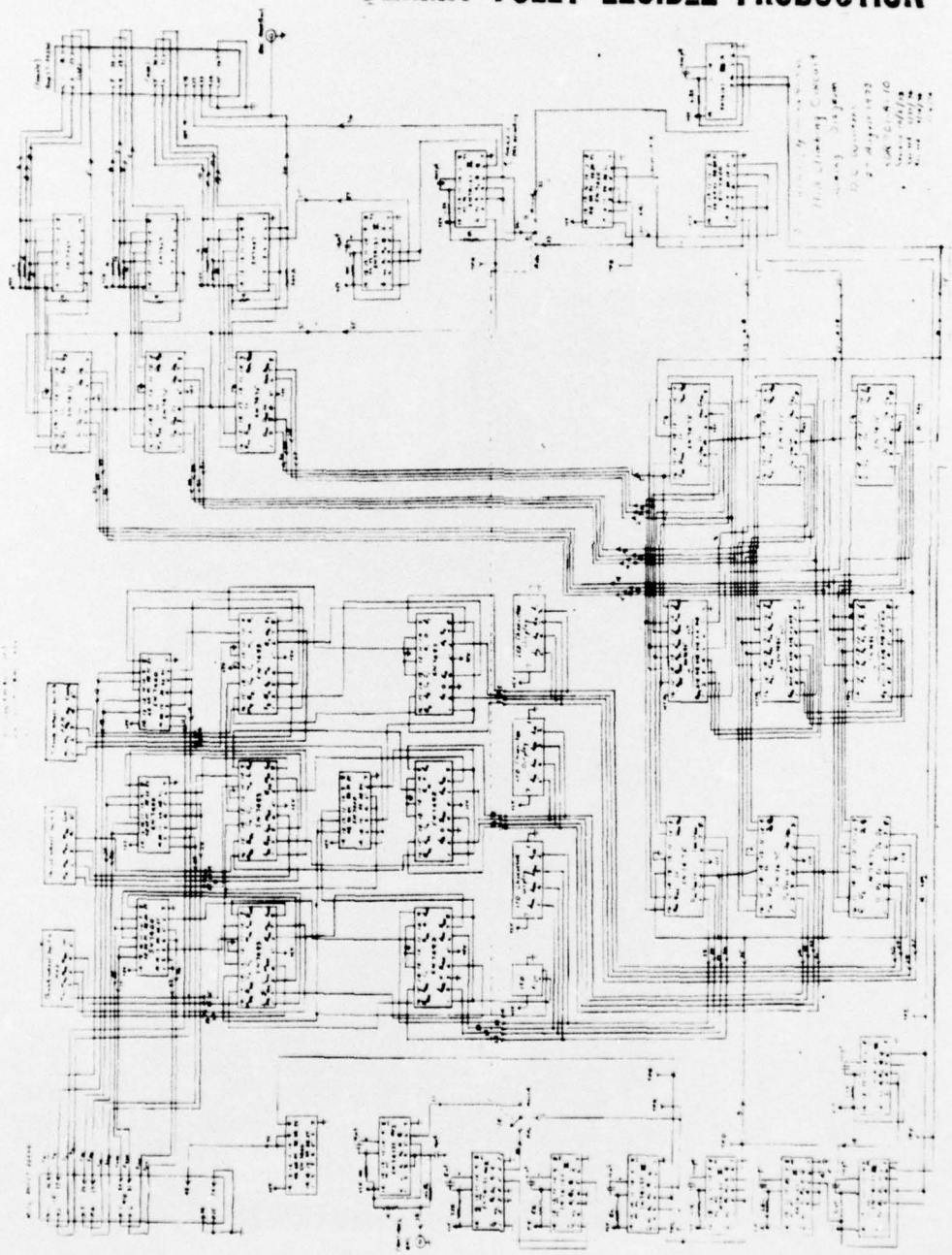

Figure 5. Back board wiring by connector numbers.

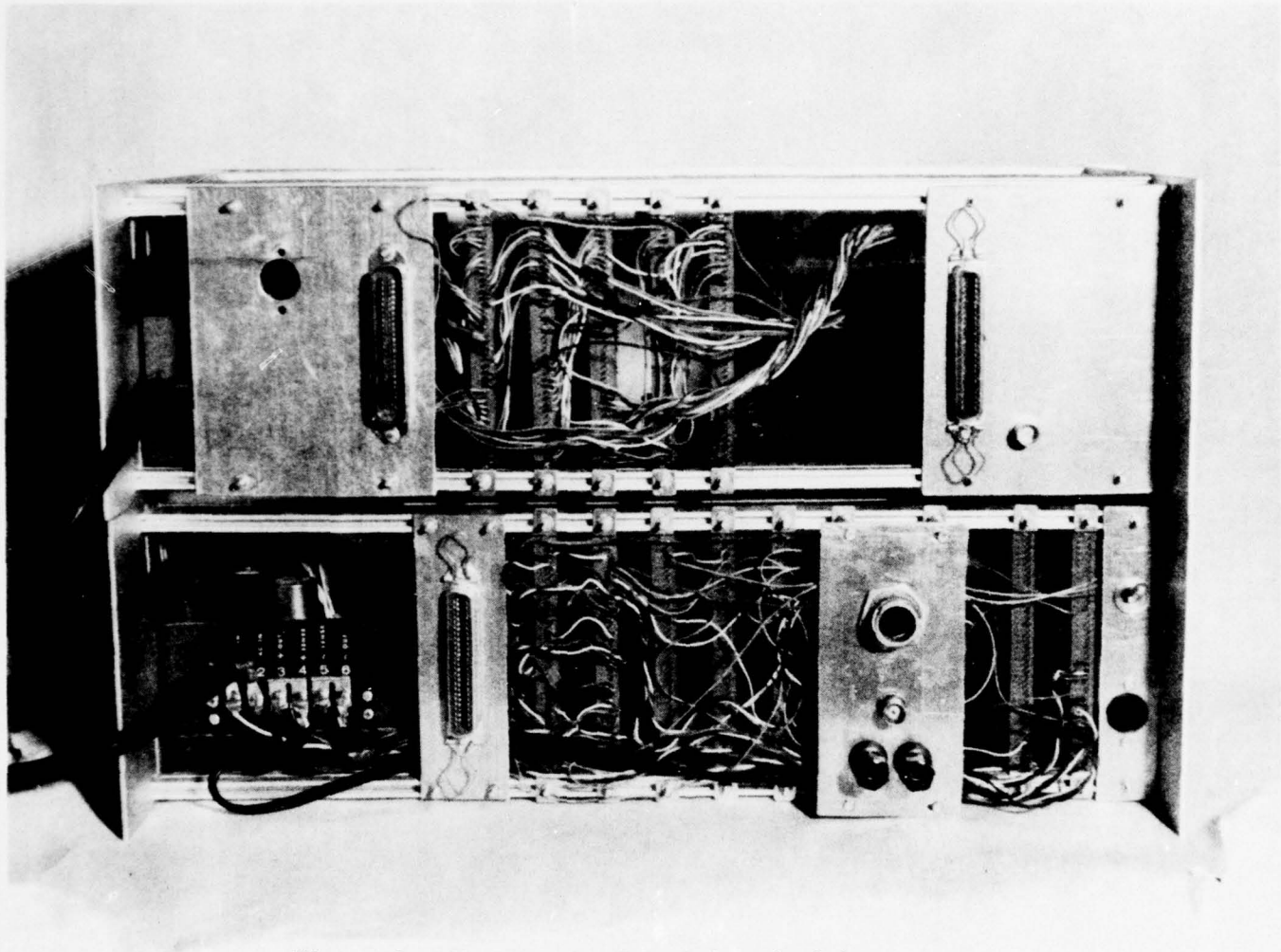

Figure 6. Photograph of back board wiring.

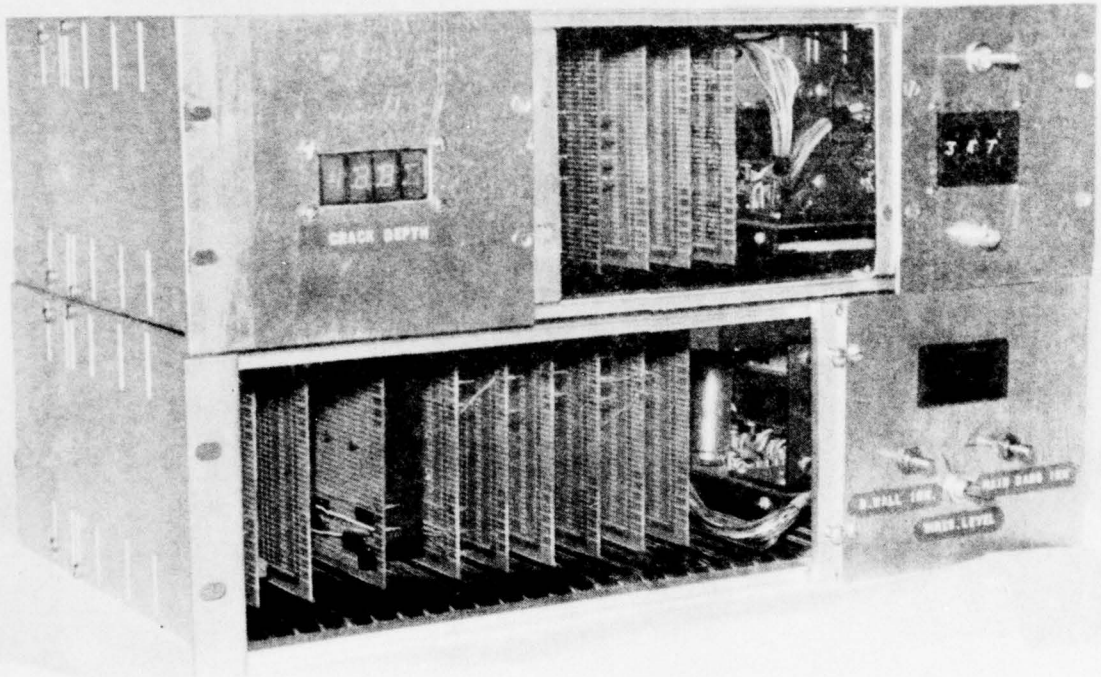

Figure 7. Photograph of front panel layout.

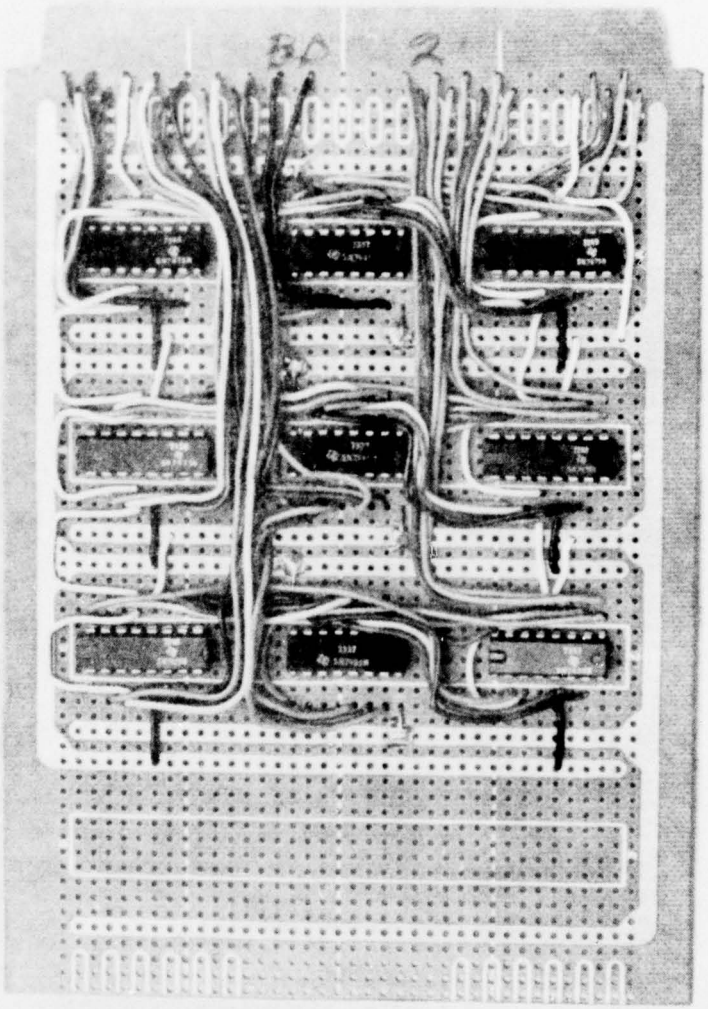

Figure 8. Photograph of comparator circuit board.

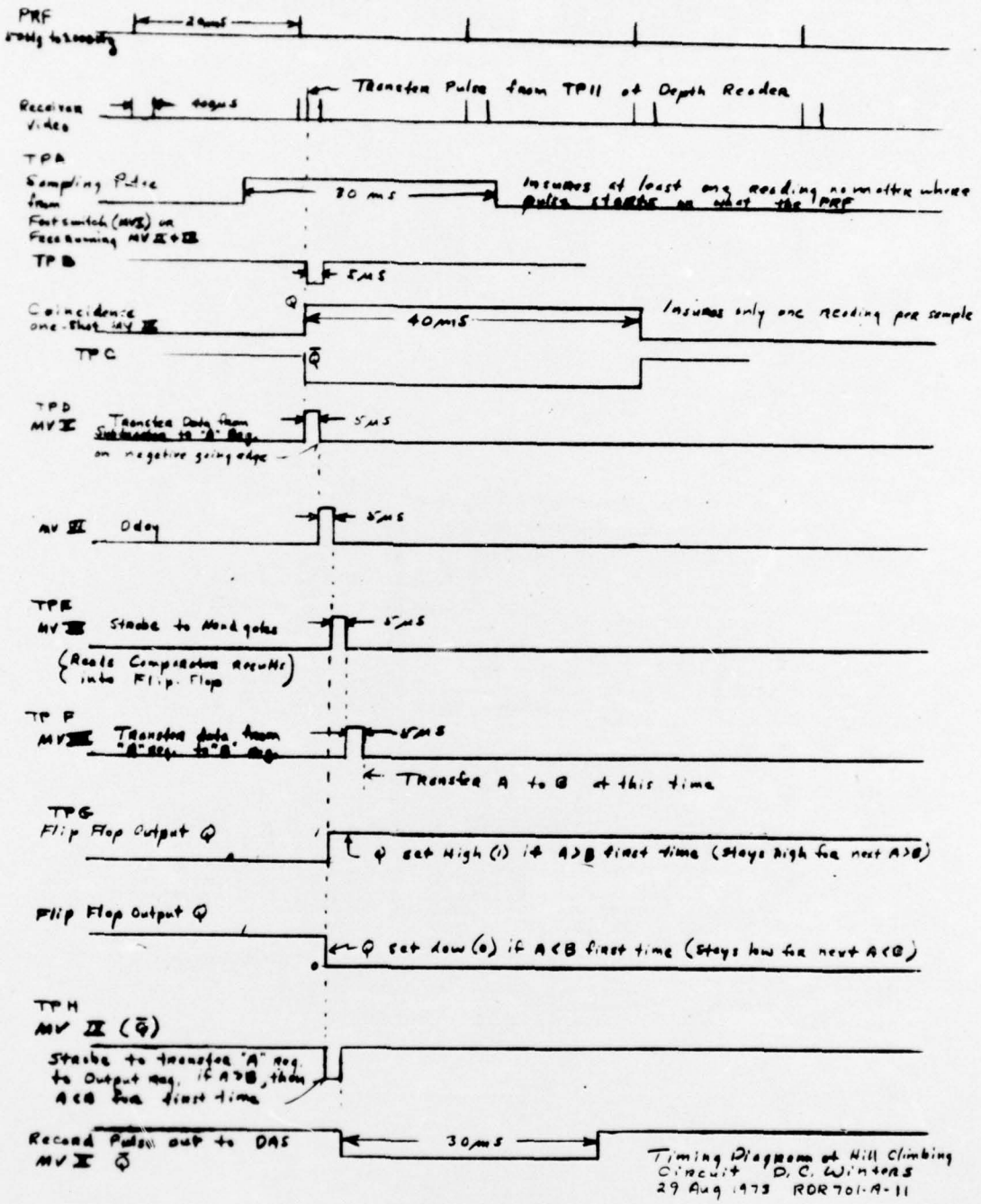

Figure 9. Timing diagram.

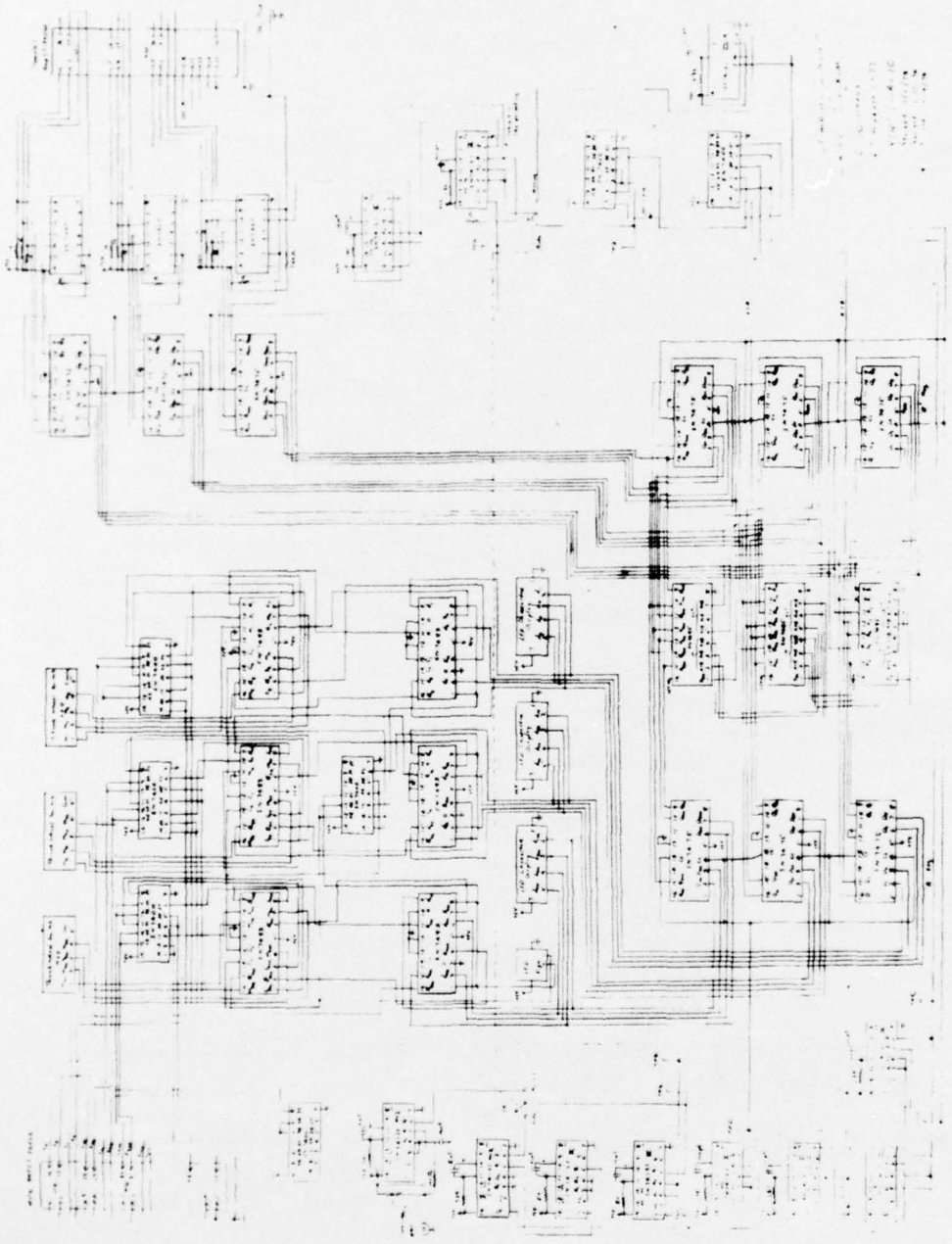

Figure 10. Detailed wiring diagram of Hill Climbing Circuit.

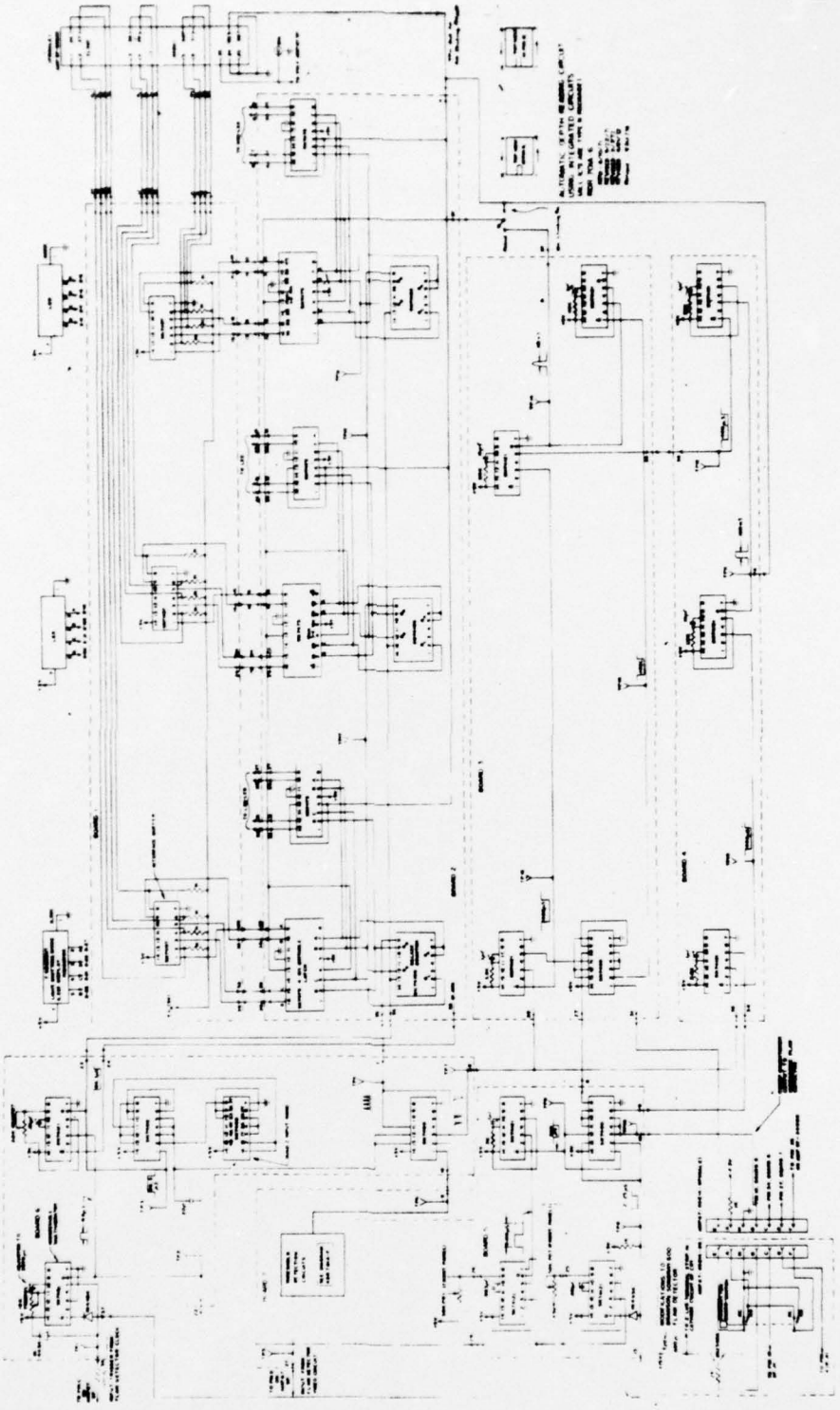

Figure 11. Modified wiring diagram of crack tip measurement circuit.